What is claimed is:

1. A method for aligning clock signals, the method comprising the steps of:

a) receiving first and second clock signals by respective first and second logic circuitry, wherein the first and second clock signals are substantially synchronized and operations of the first logic circuitry and second logic circuitry are clocked by the respective first and second clock signals;

b) receiving, by the first logic circuitry, a third clock signal, wherein the third clock signal is derived from the second clock signal;

c) repeatedly sampling the third clock signal with the first clock signal, using the first logic circuitry;

d) detecting relative phase relations of the first and third clock signals repeatedly by the first logic circuitry; and

e) altering the phase of the third clock signal responsive to an accumulation of the phase relation detecting.

2. The method of claim 1, wherein step e) includes altering the phase responsive to the accumulated detections indicating that the first and third clock signals are more often out-of-phase with one another than in-phase.

3. The method of claim 1, wherein the first logic circuitry includes a state machine, a flip timer and an edge counter, and step d) comprises the steps of:

latching certain signals for the state machine in cycles of logic operations responsive to a certain edge of the first clock, wherein the certain signals include the state machine's own initial state in a cycle, an external signal, a timer value output by the flip timer, and an edge counter signal output by the edge counter;

asserting a count signal by the state machine if the machine requires the flip timer or edge counter to count; and

asserting a flip signal by the state machine if the machine indicates an adjustment of phase..

4. The method of claim 3, comprising the steps of:

ending in the idle state for a logic cycle of the state machine if an initial state of the machine for the logic cycle is idle and the external signal is not asserted;

ending in the count state for the logic cycle of the state machine if the initial state of the machine for the logic cycle is idle and the external signal is asserted;

ending in the count state for the logic cycle of the state machine if the initial state of the machine for the logic cycle is the count state and the flip timer value is greater than zero;

ending in the flip state for the logic cycle of the state machine if the initial state of the machine for the logic cycle is the count state and the flip timer value is zero and the edge counter count value has reached a high limit; and

ending in the idle state for the logic cycle of the state machine if the initial state of the machine for the logic cycle is the count state and the flip timer value is zero and the edge counter count value has not reached a high limit.

5. The method of claim 3, wherein the first logic includes an edge detector, and step c) comprises outputting, as a detected level signal by the edge detector, the phase relation of the third clock to the first clock, wherein the third clock state is latched responsive to each one of a certain edge of the first clock.

6. The method of claim 5, wherein step d) comprises the steps of:

latching signals for the edge counter, including the count signal from the state machine and the detected level signal from the edge detector, responsive to the certain edge of the first clock for each cycle of logic operations;

resetting the edge counter to a certain middle value during a logic cycle as indicated by the count signal of the state machine.

incrementing the edge counter during the logic cycle if the count signal indicates the state machine requires counting, and the edge counter has not reached a high or low limit, and the detected level output by edge detector is high;

decrementing the edge counter during the logic cycle if the count signal indicates the state machine requires counting, and the edge counter has not reached a high or low limit, and the detected level output by edge detector is low;

holding the edge counter during the logic cycle if the count signal indicates the state machine requires counting, and the edge counter has reached a high or low limit.

7. The method of claim 3, wherein step d) comprises the steps of:

latching signals for the flip timer, including the count signal from the state machine, responsive to a certain edge of the first clock for each cycle of logic operations;

resetting the flip timer to a certain starting value during a logic cycle if the count signal indicates the state machine does not require counting down ;

decrementing the flip timer during a logic cycle if the count signal indicates the state machine requires counting down; and

holding the flip timer during a logic cycle if the count signal indicates the state machine requires counting down and the flip timer has expired.

8. The method of claim 3, wherein the second logic includes a synchronizer, and step d) comprises the steps of:

latching certain signals for the synchronizer, including the flip signal from the state machine, responsive to a certain edge of the second clock for each cycle of logic operations; and

asserting a derived clock gate output signal for the synchronizer if the flip signal indicates that the state machine indicates a phase adjustment..

9. The method of claim 8, wherein the second logic circuitry includes a clock divider, and step e) comprises the steps of:

latching, for the clock divider, the derived clock gate signal from the synchronizer responsive to a certain edge of the second clock; and

adjusting the phase of the derived clock signal if the derived clock gate signal is asserted.

10. Apparatus for aligning clock signals, the apparatus comprising:

first and second logic circuitry for receiving respective first and second clock signals, wherein the first and second clock signals are substantially synchronized and operations of the first logic circuitry and second logic circuitry are clocked by the respective first and second clock signals, wherein the first logic circuitry receives a third clock signal derived from the second clock signal, and by repeatedly sampling the third clock signal using the first, the first logic circuitry repeatedly detects relative phase relations of the first and third clock signals, and wherein the second logic circuitry adjusts the phase of the third clock signal responsive to an accumulation of the phase relation detecting.

11. The apparatus of claim 10, wherein the adjustment of phase responsive to an accumulation of the phase relation detecting includes phase adjustment responsive to the accumulated detections indicating that the first and third clock signals are more often out-of-phase with one another than in-phase.

12. The apparatus of claim 10, wherein the first logic circuitry includes a state machine, a flip timer and an edge counter, and repeatedly detecting relative phase relations comprises latching certain signals for the state machine in cycles of logic operations responsive to a certain edge of the first clock, wherein the certain signals include the state machine's own initial state in a cycle, an external signal, a timer value output by the flip timer, and an edge counter signal output by the edge counter; and wherein the state machine asserts a count signal if the machine requires counting and asserts a flip signal if the machine requires an adjustment of phase.

13. The apparatus of claim 12, wherein the state machine ends i) in an idle state for a logic cycle if an initial state of the machine for the logic cycle is idle and the external signal is not asserted, ii) in a count state for the logic cycle if the initial state of the machine for the logic cycle is idle and the external signal is asserted, iii) in a count state for the logic cycle if the initial state of the machine for the logic cycle is the count state and the flip timer value is greater than zero, iv) in a flip state for the logic cycle if the initial state of the machine for the logic cycle is the count state and the flip timer value is zero and the edge counter count value has reached a high limit, and v) in the idle state for the logic cycle if the initial state of the machine for the logic cycle is the count state and the flip timer value is zero and the edge counter count value has not reached a high limit.

14. The apparatus of claim 12, wherein the first logic includes an edge detector, and repeatedly sampling the third clock using the first clock comprises outputing by the edge detector, as a detected level signal, the state of the third clock, wherein the third clock state is latched responsive to each instance of a certain edge of the first clock.

15. The apparatus of claim 14, wherein detecting relative phase relations of the first and third clocks comprises latching signals for the edge counter, including the count signal from the state machine and the detected level signal from the edge detector, responsive to the certain edge of the first clock for each cycle of logic operations, resetting the edge counter to a certain middle value during a logic cycle if the count signal indicates the state machine does not require counting, incrementing the edge counter during the logic cycle if the count signal indicates the state requires counting and the edge counter has not reached a high or low limit and the detected

level output by edge detector is high, decrementing the edge counter during the logic cycle if the count signal indicates the state machine requires counting and the edge counter has not reached a high or low limit and the detected level output by edge detector is low, and holding the edge counter during the logic cycle if the count signal indicates the state machine requires counting, and the edge counter has reached a high or low limit.

16. The apparatus of claim 12, wherein detecting relative phase relations of the first and third clocks compriseslatching signals for the flip timer responsive to a certain edge of the first clock for each cycle of logic operations, including the count signal from the state machine, resetting the flip timer to a certain starting value during a logic cycle if the count signal indicates the state machine does not require counting, decrementing the flip timer during a logic cycle if the count signal indicates the state machine requires counting and the flip timer has not expired, and holding the flip timer during a logic cycle if the count signal indicates the state machine requires counting and the flip timer has expired.

17. The apparatus of claim 12, wherein the second logic includes a synchronizer, and detecting relative phase relations of the first and third clocks comprises latching certain signals for the synchronizer responsive to a certain edge of the second clock for each cycle of logic operations, wherein the certain signals include the flip signal from the state machine, and asserting a derived clock gate output signal for the synchronizer if the flip signal indicates that the state machine requires a phase adjustment of the derived clock..

18. The apparatus of claim 17, wherein the second logic circuitry includes a clock divider, and phase adjustment of the third clock signal comprises latching, for the clock divider, the derived clock gate signal from the synchronizer responsive to a certain edge of the second clock, and gating of the derived clock signal if the derived clock gate signal is asserted.

19. Apparatus for aligning clock signals, the apparatus comprising:

first and second logic circuitry for receiving respective first and second clock signals, wherein the first and second clock signals are substantially synchronized and operations of the first logic circuitry and second logic circuitry are clocked by the respective first and second clock signals, wherein the first logic circuitry includes a state machine, a flip timer, an edge counter and edge detector, and receives a third clock signal derived from the second clock signal, wherein by repeatedly sampling third clock signal with the first, the first logic circuitry repeatedly detects relative phase relations of the first and third clock signals, and wherein the second logic circuitry includes a clock divider and a synchronizer, and the second logic circuitry adjust the phase of the third clock signal responsive to an accumulation of the phase relation detecting, and wherein phase adjustment of the third clock signal comprises latching, for the clock divider, a signal from the synchronizer responsive to a certain edge of the second clock, and phase adjustment of the derived clock signal if the signal from the synchronizer is asserted.

20. The apparatus of claim 19, wherein detecting relative phase relations of the first and third clocks comprises latching signals for the edge counter, including a count signal from the state machine and a detected level signal from the edge detector, responsive to the certain edge of the first clock for each cycle of logic operations, resetting the edge counter to a certain middle value during a logic cycle if the count signal indicates the state machine does not require counting, incrementing the edge counter during the logic cycle if the count signal indicates the state machine requires counting and the edge counter has not reached a high or low limit and the detected level output by edge detector is high, decrementing the edge counter during the logic cycle if the count signal indicates the state machine requires counting and the edge counter has

not reached a high or low limit and the detected level output by edge detector is low, and holding the edge counter during the logic cycle if the count signal indicates the state machine requires counting, and the edge counter has reached a high or low limit.